Global journal of multidisciplinary and applied sciences
Available online at www.gjmas.com
©2015 GJMAS Journal-2015-3-3/76-81
ISSN **2313-6685** ©2015 GJMAS

Novel LOW POWER CNTFET Based COMPRESSOR CELL Design

Ahmad Bahmaei[1*] , Habib Rostami[2] and Ali reza Mallahzadeh[2]

1. Department Of Electrical and Electronic Engineering, Islamic Azad University, Bushehr Branch, Bushehr, Iran
2. Computer eng. Department, School of engineering, Persian gulf University, Bushehr, Iran

***Corresponding author*: Ahmad Bahmaei**

ABSTRACT: This paper presents a new (5:2) compressor circuit capable of operating at ultra-low voltages. Its power efficacy is derived from the novel design of composite XOR-XNOR gate at transistor level. The new circuit eliminates the weak logic and threshold voltage drop problems, which are the main factors limiting the performance of pass transistor based circuits at low supply voltages. The proposed (5:2) compressor has been designed with special consideration on output drivability to ensure that it can function reliably at low voltages when these cells are employed in the tree structured multiplier and multiply accumulator. Simulation results show that the proposed *(5:2)* a novel CNTFET compressor cell will be increases all the arithmetic logic unit performance is presented. In this paper, We present a new compressor cell design using carbon nanotube field effect transistors (CNTFETs). In the design we have 10 transistors and so that we have achieved an improvement in the output parameters. Simulations were carried out using HSPICE based on the CNTFET model with 0.9V VDD. The denouements results in that we have a considerable improvement in power, Delay and power delay product than the CMOS full adder index terms_ compressor, CMOS, CNTEFT

***Keywords*:** Low Power, Compressor, Cell.

INTRODUCTION

Fast arithmetic computation cells including adders and multipliers are the most frequently and widely used circuits in VLSl systems. Microprocessors and digital signal processors rely on the efficient implementation of generic arithmetic logic units and floating point units to execute dedicated algorithms such as convolution and filtering [l-41. In most of these applications, multipliers have been the critical and obligatory component dictating the overall circuit performance when constrained by power consumption and computation speed. With trends of VLSl technologies towards deep-submicron regime, the most eminent means of achieving power efficacy is high Lowering the power supply voltage. Therefore, it is imperative to explore circuit design techniques to achieve high power efficacy of arithmetic circuits at ultra-low supply voltages. Fast multipliers are generally composed of three sub functions: *partial product generation, partial product accumulation* and *carry-propagating addition*. In the partial product generation circuit, Booth encodings are often

Used to reduce the number of partial products. A summation tree, called the Carry Save Adder (CSA) tree, is used in the second function to further reduce the partial products to two. The last function is normally fulfilled by the fast cany propagate adder, such as canny look-ahead adder and canny-skip adder. Early designs of CSA tree use the (3:2) counters, or full adders for the partial product accumulation, in which 3 equally weighted bits were combined to produce two output bits. The (4~2) compressors, due to their ability to form regular interconnected cells structure, are more popularly used nowadays. Higher input compressors such as *(5:2),* (6:2), etc., have also been studied and increasingly employed in high precision multipliers to achieve greater performance. There has been an increasing interest to use fast (5:2) compressor for large ward-sire multiplier and multiply accumulators [I, 21. In this paper, we investigate several fast *(5 2)* compressor architectures and devise a new circuit that built around composite XOR-XNOR gates and multiplexers. Various CMOS logic styles for implementing these primitive cells at transistor level have been studied and a new design is proposed. The proposed fast (5:2) compressor architecture designed with

the new composite gate and multiplexer cells is able to operate he low 1 volt with fJ power efficacy. Meantime, the driving capability is assured by simulating the circuit in an environment similar to its use in a tree structured accumulator.

2. (5 2) COMPRESSOR ARCHITECTURES

The block diagram of a *(5:2)* compressor is shown in Fig. I , which has seven inputs and four outputs. Five of the inputs are the primary inputs x,, x2, *x,,* x4 and .q, and the other two inputs, cnl and c,"> receive their values from the neighboring compressor of one binary bit order lower in significance. All the seven inputs have the same weight. The *(5 2)* compressor generates an output, *sum* of the same weight as the inputs, and three outputs, *Carty, cDUtal* nd *couf2*w weighted one binary order higher. The cull and coUo are fed to the neighboring compressor.

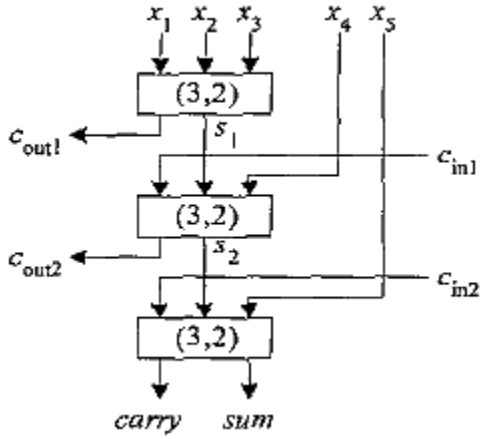


Figure 1. Black diagram

A simple implementation of the *(5 2)* compressor is to cascade three (3,2) parallel counters in a hierarchical structure, as shown in Fig. 2. Since a (3,2) parallel counter is equivalent to a full adder, this architecture has a critical path delay of 64,,, where A,,, is the delay of an XOR gate. A faster (5:2) compressor is shown in Fig. 3. This architecture is proposed in [I],w hich uses a different method to generate cOualln d *c,.,~*. It is claimed to have a delay of 4A,,,. Fig. 4 shows another architecture of a *(5 2)* compressor [2]. Careful analysis shows that this design has a critical path delay of 4A,,, +Amu as oppose to SAx,, reported in *[2]*. The style and structure of the circuit share some common attributes as the recently published structural design of full adders [4,5] and (4:2) compressors *[2,6]*.

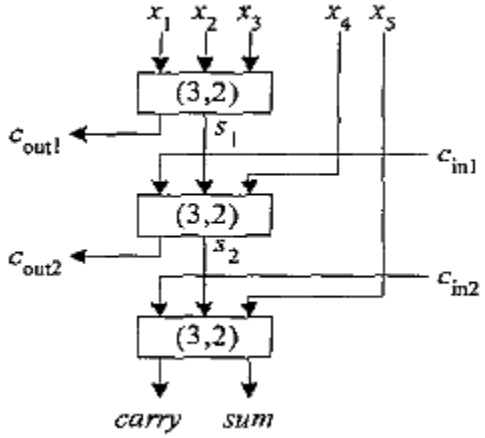


Figure *2. (5:2)* compressor based on cascaded *(3,2)* counters

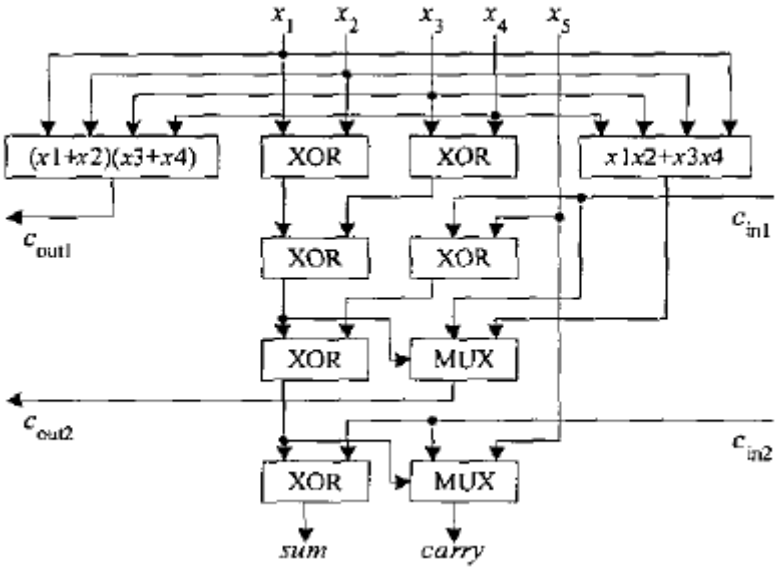


Figure 3. *(5:2)* compressor architecture of [l]

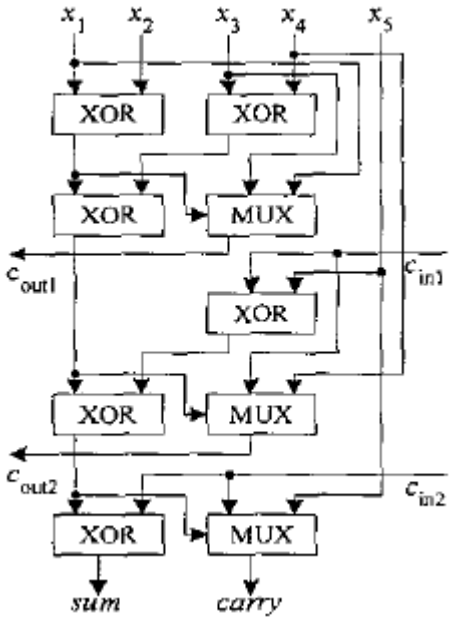


Figure 4. *(5 2)* compressor architecture of [2]

In spite of structural differences of various implementations, the formulae to generate the output signals are essentially derived from the basic architecture of Fig. 2. Each full adder can be logically expressed as:

S = x´y´z + x´yz´ + xy´z´ + xyz (1)

C = xy + xz + yz (2)

where *a, b,* and *c* are the primary inputs and sFA and *C F* a~re the primary outputs of the full adder. It follows that the outputs and the internal nodes of Fig. 2 can be expressed by the following set of equations. Based on the above formulae, it is conjectured that lowering the critical path delay of the (5:Z) compressor to 3A,,, or lower is almost impossible. However, it is very likely to explore different logic design styles at transistor level to achieve significantly improved low power and high-speed *(5 2)* compressor cells for instantiation at architectural level. For example, a dual rail *(5:2)* compressor [2] is proposed for the architecture of Fig. 4, where the XOR gates are implemented as dual rail multiplexers to improve the performance.

3. PROPOSED CIRCUITS LEVEL DESIGN

Having defined the notion of the *(5:2)* compressor, our objective is to develop novel circuits at transistor level that leverage on advanced CMOS technologies to realize a low voltage, low power *(5 ~ 2)* compressor cell with sustainable speed and acceptable area cost. It is obvious from Fig. *3* and 4 that the primitive logic elements are XOR-XNOR gate and multiplexer. Since the compressors are normally cascaded in tree structure to reduce the height of the partial product matrix, it is imperative that the outputs of the compressor have enough drivability. Fig. *5* shows three circuit implementations of the composite XOR-XNOR cell. Circuit (a) consumes very low power [4]. However, it generates a weak logic '1' when the primary inputs are ' 11 ' , which prevents it from functioning reliably at low supply voltages. Circuit (b) is able to operate at low voltages, but it is not power efficient [4]. Both Circuits (a) and (b) use inverter to generate the xor/xnor signals. Therefore, the outputs of these complimentary signals are heavily skewed in time. Fig. S(c) shows the schematic and layout of our proposed XORXNOR cell. The output signals are generated simultaneously with balanced delay. It is able to operate under very low voltages because the weak logic problem caused by the pass transistors is circumvented by the pair of feed-back transistors. Fig. 6 shows the circuit implementation of a simple XOR gate and its layout. It is used in some blocks of the architecture of Fig. 4 where only the exclusive-or output is needed.

4. CNTFET

As one of the hopeful new devices, CNTFET avoids many of conventional silicon devices limitation [4]. All the carbon atoms in CNT are bonded to each other and there is no hanging bond which enables the combination with high- k dielectric materials. A carbon atom in grapheme assembles in a single-sheet hexagonal lattice. In this paper we use single-walled carbon Nano-tube (SWCNT) which can Be observed as a graphite sheet is rolled up and attach together along a wrapping vector $C_h = n_1 \cdot \bar{a}_1 + n_2 \cdot \bar{a}_2$ where $[\bar{a}_1, \bar{a}_2]$ are lattice unit vectors , and the index (n1, n2) are positive integers that identify the chirality's of the tube[5]. Length of Ch is thus the circumference of the CNT, which is given by 1-1.

$$C_h = a\sqrt{n_1^2 + n_1^2 + n_1 n_2} \quad (3)$$

Single-walled CNTs are classified into one of their groups, depends on the chiral number (n1, n2): (1) armchair (n1 = n2), (2) zigzag (n1 = 0 or n2 = 0), and (3) Chiral (all other indices) and here we use CNT with the chiral number (19, 0). The electrons in CNT are restricted within the atomic plane of grapheme. Due to the quasi-1D structure of CNT, the motion of the electrons in the Nano-tubes is extremely limited. Single electrons may move freely along the tube axis direction. As a result, all wide angle scatterings are prohibited. Only forward scattering and back scattering due to electron phonon interactions are possible for the carriers in Nano-tubes. The operation principle of Carbon Nano-tube Field Effect Transistor (CNTFET) is similar to the conventional silicon devices. This three (or four) terminal device consists of a Semi-conducting Nano-tube, acting as conducting channel, bridging the source and drain contacts. The device is turned on or off electrostatically through the gate. The quasi-1D device structure provides better control of electrostatic gate above the channel distraction than 3D and 2D device structures. In terms of the device operation mechanism, CNTFET can be grouping as either Schottky Barrier (SB) controlled FET (SB-CNTFET) or MOSFET-like FET [4]. The conductivity of SB-CNTFET is controlled by the majority carriers tunneling via the SBs at the end contacts. The On-current and consequently device performance of SB-CNTFET is determined by the contact resistance due to the existence of tunneling barriers at both or one of the source and drain contacts, instead of the channel conductance. SB-CNTFET exhibits am bipolar transport behavior [6]. The work function induced obstacles at the end contacts can be made to increase either electron or hole transport. As a result both polar device (N-type FET or P-type FET) and the device bias point can be adjusted by choosing the appropriate work function of source/drain contacts. On the other hand, MOSFET like CNTFET exhibits unipolar behavior by blocking either electron (pFET) or hole (nFET) transport with deeply doped source/drain [6]. The non-tunneling potential barrier in the channel region, and thus the conductivity, is modulated by the gate-source bias. Although better dc current can be obtained by SB-CNTFET with the self- aligned structure, its efficiency is going to be poor due to the nearness of the gate electrode to the source/drain metal. The am bipolar behavior of SBCNTFET also makes it undesirable for complementary logic design. Taking into account both the manufacture achievability and superior performance of MOSFET-like CNTFET as compared to SB-CNTFET, the CNTFET that used in HSPICE model is MOSFET-like CNTFET.

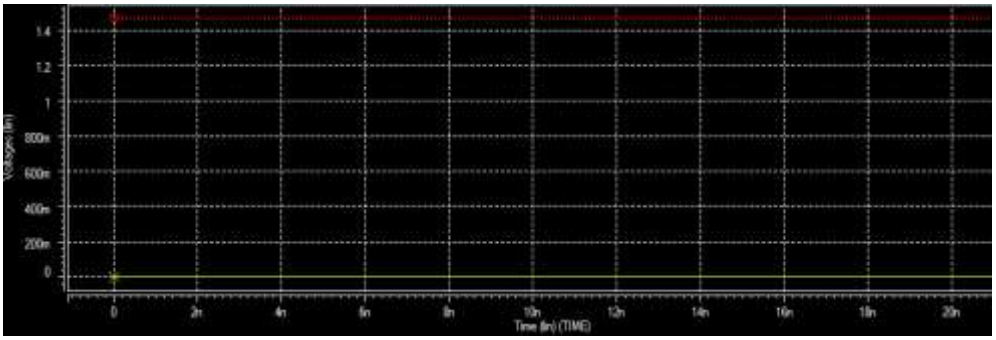
5. SIMULATIONS AND ANALYSIS

In this paper, we presented a CNT based full adder cell witch shown in figure 1. This full adder simulated in H_SPICE 2007. CNT parameters witch used for simulation are in table 1. The outputs of this circuit are completely full swing (As shown in Figure 5). Finally, the calculated result of PDP, delay and power parameters is proposed in table 2. Our proposed circuit power

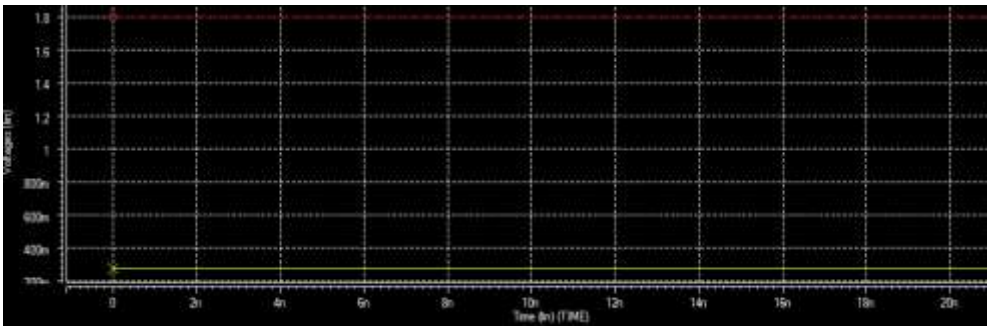
and delay are less than CMOS full adder circuit. Table 3 shows Compressor implementation for CMOS and CNTFET implementation results summery.

Table1. CNT simulation parameters.

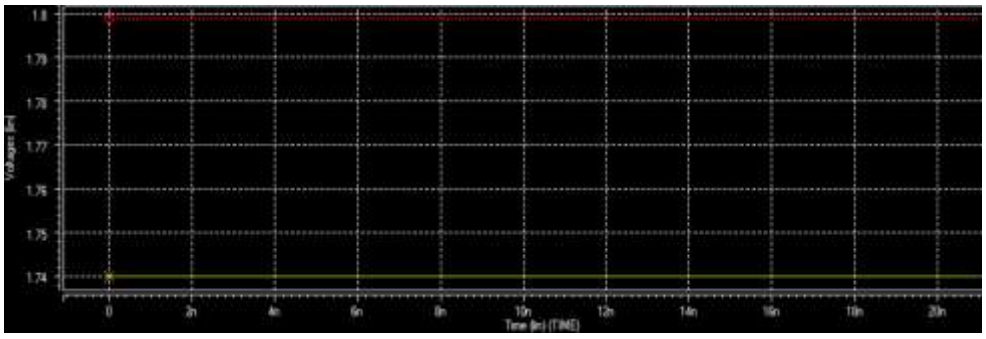
Param	Value	Param	Value
INGOLD	2	DCON	1
GSHUNT	1e-12	RMIN	1e-15
ABSTOL	1e-5	ABSVDC	1e-4
RELTOL	1e-2	RELVDC	1e-2
NUMDGT	4	PIVOT	13
TEMP	25	Ccsd	0
CoupleRatio	1	Efo	0.6
Wg	0	Cb	40e-12
Lg	32e-9	Lgeff	100e-9
Vfn	0	Vfp	0
m	13	N	0
Hox	4e-9	Kox	16



5(a).simulation for (A=1,B=1,C=0), Carry and sum are red and yellow respectively.



5(b).simulation for (A=1,B=0,C=1), Carry and sum are red and yellow respectively.



5(c).simulation for (A=1,B=1,C=1), Carry and sum are red and yellow respectively (SUM=1.74, Carry=1.8). Figure 5. Fig5. Simulation results (A, B, Cin, Sum, Cout)

Table 2. Simulation results (A, B, Cin, Sum, Cout)

DESIGN	TECHNOLOGY	VOLTAGE	POWER	DELAY	THD	PDP
CMOS	180nm	1.8V	40.55pW	0.01e-6 S	75.47%	0.1452e-18 J
CNT	CNTFET	1.8V	1pW	0.01e-12S	79.01%	1.05e-21J

Table 3. Compressor implementation design summery

Compressor	Power(W)(all inputs are active)	Delay(s)	PDP(J)
CMOS	153.24p	0.01	1.5324p
CNTFET	4.12n	0.0025	.0103n

CONCLUSION

Various architectures of (5:2) compressor are analyzed. Different CMOS logic design styles for implementing the primitive modules of the compressor at transistor level are explored. Two new circuits are proposed, one for the complex logic gate to co-generate the XOR-XNOR outputs and the other for the multiplexer. A regular layout and cascadable novel (59) compressor is constructed from these composite gate and multiplexer circuits. Simulation results show that the new (52) compressor is capable of functioning down to 0.7V, and still maintain superior power efficacy. Therefore, it is an excellent cell library component to realize future high-speed, low power arithmetic logic unit at sub-IV supply voltages.

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